REMARKS

The Office Action dated January 25, 2005 (Paper No. 20050121) has been received and the Examiner's comments carefully reviewed. Prior to entry of this paper, Claims 1-20 were pending. Claims 1-6, 8-13, 17, and 20 were rejected. Claims 7, 14-16, 19, and 19 were objected to, but were identified as being allowable if re-written in independent form. In this paper, Claims 13 and 20 are amended to correct clerical errors, and Claims 21-29 are added. Claims 1-29 are currently pending. No new subject matter has been added. For at least the following reasons, Applicants respectfully submit that each of the presently pending claims is in condition for allowance.

Rejection to Claims 13 under 35 U.S.C. §112

Claim 13 was rejected as being anticipated under 35 U.S.C. § 112, second paragraph. Claim 13 was amended to correct a clerical error. It is respectfully submitted that the rejection to Claim 13 is moot in light of the amendment to Claim 13, and notice to that effect is earnestly solicited.

Rejection to Claims 1, 3-6, 8-13, 17, and 20 as being anticipated by Yamauchi

Claims 1, 3-6, 8-13, 17, and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yamauchi. Applicants respectfully traverse the rejection.

It is respectfully submitted that the rejection to Claim 1 should be withdrawn at least Yamauchi does not disclose "a first variable resistance circuit" and "a second variable resistance circuit", as recited in Applicants' Claim 1.

In Yamauchi, a driver 10 outputs a current to a cable 20 having a characteristic impedance Z_0. Two signal lines of the cable 20 are coupled, through respective terminating resistor Rt, to a bias voltage Vm. (See Yamauchi, col. 3, lines 19-30). Driver 10 includes transistor 11, which provides current Idp, and transistor 14, which provides current Idn. The gate voltage control circuit 30 prevents drain currents Idp and Idn from varying in spite of changes to the drain-to-source voltages of transistors 11 and 14. This ensures that a constant current is output to cable 20. (See Yamauchi, Col. 4, lines 7-23).

In contrast, the Applicants' Claim 1 recites "a first variable resistance circuit" and "a second variable resistance circuit. The Office Action states that "the recited first and second variable resistance circuits reads on FETs 11 and 14 respectively". Applicants respectfully disagree. Transistor 11 of Yamauchi is biased as a current source, not as a variable resistance circuit. Transistor 14 of Yamauchi is biased as a current sink, not as a variable resistance circuit.

Also, it is respectfully submitted that the rejection to Claim 1 should be withdrawn at least because Yamauchi does not disclose "a feedback circuit that is coupled to the first and second variable resistance circuits, wherein a source resistance of the output driver circuit appears to a load as substantially similar to a termination resistance of the load", as recited in Applicants' Claim 1. Further, it is respectfully submitted that the rejection to Claim 3 should be withdrawn at least because Yamauchi does not disclose "the feedback circuit is configured to adjust the first variable resistance circuit and the second variable resistance circuit to track a change in the termination resistance, such that the source resistance tracks the change in the termination resistance", as recited in Applicants' Claim 3.

The Office Action states, "The limitation on the last two lines of claim 1 is deemed to be inherent in the operation of Yamauchi's Fig. 1 circuit (because it is the object of Yamauchi to match the output impedance of driver 10 to the load which is to be coupled to line 20). The same is true for the limitation of Claim 3." Applicants respectfully disagree. In Yamauchi, the feedback circuit does not adjust the source resistance. Gate voltage control circuit 30 of Yamauchi is arranged to control voltage Vgp such that current Idp is fixed regardless of changes in voltage Vm. (See Yamauchi, col. 3 lines 14-20.) Similarly, gate voltage control circuit 30 of Yamauchi is arranged to control voltage Vgp such that current Idn is fixed regardless of change in voltage Vm. Although the output **voltage** provided to driver 10 of Yamauchi may be changed by changes to currents Idp and Idn, the source **resistance** is not affected by changes in currents Idp and Idn. The source resistance is not affected by changes in voltages Vgp and Vgn of Yamauchi.

For at least these reasons, it is respectfully submitted that the rejection to Claims 1 and 3 be withdrawn.

It is respectfully submitted that the rejection should be withdrawn with regard to Claims 17 and 20 at least for reasons similar to those stated above with regard to Claim 1. Further, it is

respectfully submitted that the rejection should be withdrawn with regard to Claims 3-6 and 8-13 at least because they depend from Claim 1.

Additionally, it is respectfully submitted that the rejection should be withdrawn with regard to Claim 6 because Yamauchi does not disclose, "the feedback circuit is configured to adjust an on-resistance that is associated with the transistor", as recited in Applicants' Claim 6. As is well known in the art, a MOSFET biased in the linear region of operation behaves approximately like a resistor having an on-resistance that is approximately inversely proportional to V_{GS}-V_T. However, in the saturation region, rather than behaving like a resistor, a MOSFET provides a drain current that is approximately proportional to $(V_{GS}-V_T)^2$, and behaves approximately as a current source or current sink rather than as a resistor. Because transistor M84 of Yamauchi is biased in saturation mode rather than linear mode, the feedback does not "adjust an on-resistance that is associated with the transistor."

Rejection to Claims 1-3, 5, 6, 8, 9, 12, 13, 17, and 20 as being anticipated by Macaluso

Claims 1-3, 5, 6, 8, 9, 12, 13, 17, and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by Macaluso et al, USPN 6,380,797 (herein referred to as Macaluso). Applicants respectfully traverse the rejection.

It is respectfully submitted that the rejection to Claim 1 should be withdrawn at least Macaluso does not disclose "a first variable resistance circuit" and "a second variable resistance circuit", as recited in Applicants' Claim 1.

Referring to FIG. 2 of Macaluso, current source 104 is used to set the current flowing through current sink transistor M84 so that the current through M84 is m*(1.25/R34). (See Col. 5, lines 54-64 of Macaluso.) This current is used to set the voltage swing of the output swing 201-204 to 800mV, virtually constant regardless of PVT. (See Col. 5, line 64 through Col. 6, line 22 of Macaluso). Output driver 102 uses the output swing to provide output signal 120. Since the output swing is constant across PVT, the output signal 120 is also independent of PVT. (See Col. 5, lines 1-4 of Macaluso). Replica bias circuit 103 and source follower M94 are used to keep the output offset (VOS) of output signal 120 at a fixed value of 1.2V. (See Col. 7, lines 1-21 of Macaluso).

In contrast, Applicants' Claim 1 recites "a first variable resistance circuit" and "a second variable resistance circuit". The Office Action states that "the recited first and second variable resistance circuits reads on FETs M94 and M84 respectively". Applicants respectfully disagree. Transistor M94 of Macaluso is biased as a source follower, not as a variable resistance circuit. (See Col. 6, lines 44-48 of Macaluso.) Transistor M84 of Macaluso is biased as a current sink, not as a variable resistance circuit. (See FIG. 2 of Macaluso.)

Also, it is respectfully submitted that the rejection to Claim 1 should be withdrawn at least because Macaluso does not disclose "a feedback circuit that is coupled to the first and second variable resistance circuits, wherein a source resistance of the output driver circuit appears to a load as substantially similar to a termination resistance of the load", as recited in Applicants' Claim 1. Further, it is respectfully submitted that the rejection to Claim 3 should be withdrawn at least because Macaluso does not disclose "the feedback circuit is configured to adjust the first variable resistance circuit and the second variable resistance circuit to track a change in the termination resistance, such that the source resistance tracks the change in the termination resistance", as recited in Applicants' Claim 3.

The Office Action states, "The limitation on the last two lines of claim 1 is deemed to be inherent in the operation of Macaluso's Fig. 2 circuit. The same is true for the limitation of Claim 3." Applicants respectfully disagree. In Macaluso, the source resistance does not the track termination resistance. In Macaluso, the current provided by transistor M92 may be adjusted to keep the differential output voltage constant. The **current** is adjusted to keep the **voltage** constant, but the source **resistance** remains substantially unchanged. The source resistance does not track the termination resistance. Further, because the termination resistance can change without the source resistance tracking it, the source resistance does not appear to the load as substantially similar to the termination difference.

For at least these reasons, it is respectfully submitted that the rejection to Claims 1 and 3 be withdrawn.

It is respectfully submitted that the rejection should be withdrawn with regard to Claims 17 and 20 at least for reasons similar to those stated above with regard to Claim 1. Further, it is

respectfully submitted that the rejection should be withdrawn with regard to Claims 2, 5, 6, 8, 9, 12, and 13 at least because they depend from Claim 1.

Additionally, it is respectfully submitted that the rejection should be withdrawn with regard to Claim 6 because Macaluso does not disclose, "the feedback circuit is configured to adjust an on-resistance that is associated with the transistor".

New Claims 21-29

Claim 21 is respectfully submitted to be allowable at least because it depends on Claim 1, which is proposed to be allowable. Additionally, Claim 22 is respectfully submitted to be allowable at least because it depends on Claim 17, which is proposed to be allowable. Claim 23 is respectfully submitted to be allowable at least because it depends on Claim 20, which is proposed to be allowable.

Claim 24 is respectfully submitted to be allowable at least because the prior art of record does not disclose "a first variable resistance circuit", "a second variable resistance circuit", or "a feedback circuit that is configured to control a resistance that is associated with the first variable resistance circuit and a resistance that is associated with the second variable resistance circuit such that a source resistance of the output driver circuit tracks the termination resistance", as recited in Applicants' Claim 24.

Claims 25-29 are respectfully submitted to be allowable at least because they depend on Claim 24, which is proposed to be allowable.

Additionally, Claim 28 is respectfully submitted to be allowable at least because neither Yamauchi nor Macaluso discloses, "the feedback circuit is arranged to control the resistance that is associated with the first variable resistance circuit by providing a first control signal to the gate of the transistor such that the transistor is biased in a **linear** region of operation" (emphasis added) as recited in Applicants' Claim 28.

In Macaluso, transistors M84 and M94 operate in the saturation region of operation, not the linear region of operation. (See FIG. 2 to Macaluso). Also, in Yamauchi, transistors 11 and 14 operate in the saturation region of operation. (See Figs. 2-4 and Col. 5, lines 14-33 of Yamauchi).

In Yamauchi, gate voltage Vgp is adjusted to ensure that transistor 11 remains in the saturation region operation. If gate voltage Vgp were to be held at -1.5V and the drain-to-source voltage of transistor 11 were to fall below .5V, the transistor would move into the linear region of operation, which would be undesirable because current Idp would decrease. To prevent this from happening, if the drain-to-source voltage of transistor 11 of Yamauchi falls below .5V, the gate voltage Vgp is lowered so that transistor 11 remains in the saturation region of operation. (See Col. 5, lines 14-25 of Yamauchi).

For at least the reasons stated above, it is respectfully submitted that Claims 1-29 are allowable, and notice to that effect is earnestly solicited.

Conclusion

It is respectfully submitted that each of the presently pending claims (Claims 1-29) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicant's representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

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